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1. When a _____ occurs on a line currently in the local cache, the effect depends on the current state of that line in the local cache. :-> **write hit**
2. When a _____ occurs in the local cache, the processor initiates a memory read to read the line of main memory containing the missing address. :-> **write miss**
3. When a _____ occurs on a line currently in the local cache, the processor simply reads the required item. :-> **read hit**
4. When a _____ occurs in the local cache, the processor initiates a memory read to read the line of main memory containing the missing address. :-> **read miss**
5. _____ will save time only if it is fed a stream of data from sequential locations. :-> **pipelined ALU**
6. _____ system is designed to have N independent processors that can function in parallel. :-> **parallel processor**
7. The system that is designed to address the need for vector computation is _____ :-> **array processor**
8. The _____ register contains control fields, such as vector count, that determine how many elements in the vector registers are to be processed. :-> **vector status**
9. The _____ register contains mask bits that may be used to select which elements in the vector registers are to be processed for a particular operation. :-> **vector mask**
10. _____ usually refers to an auxiliary processor attached to a general-purpose processor and used to perform vector computation. :-> **array processors**
11. To provide cache consistency on an SMP, the data cache often supports a protocol known as _____ :-> **MESI**
12. Lock manager software is limitation of _____ clustering method :-> **Servers share disks**
13. Increased complexity is limitation of _____ clustering method :-> **Active secondary**
14. High cost is limitation of _____ clustering method :-> **Passive standby**
15. Hardware-based solutions are generally referred to as _____ :-> **cache coherence protocol**
16. With a _____ protocol, there can be multiple writers as well as Multiple readers :-> **write-update protocol**
17. With a _____ protocol, there can be multiple readers but only one writer at a time :-> **write-invalidate protocol**
18. For MESI protocol, _____ is the state in which the line in the cache does not contain valid data. :-> **invalid**
19. For MESI protocol, _____ is the state in which the line in the cache is the same as that in main memory and may be present in another cache. :-> **shared**
20. For MESI protocol, _____ is the state in which the line in the cache is the same as that in main memory and is not present in any other cache. :-> **exclusive**
21. NUMA is _____ :-> **Tightly coupled**
22. SMP is _____ :-> **Tightly coupled**
23. Array processor comes under _____ stream :-> **SIMD**
24. Vector processor comes under _____ stream :-> **SIMD**
25. _____ is the benefit of active secondary clustering method :-> **Reduced cost**
26. _____ is the benefit of passive stand by clustering method :-> **Easy to implement**
27. Clusters are _____ :-> **Loosely coupled**
28. _____ is the benefit of servers share disks clustering methods :-> **Low network and Server overhead**
29. _____ is the benefit of servers connected to disks clustering Method :-> **Reduced network**
30. _____ is the benefit of separate servers clustering method :-> **High availability**
31. In _____ stream, a single machine instruction controls the Simultaneous execution of a number of processing elements on a lock Step basis :-> **SIMD**

32. In _____ stream, single processor executes a single instruction Stream to operate on data stored in a single memory :->SISD
33. SISD,SIMD,MISD,MIMD are the categories of computer systems proposed by _____ :->Flynn
34. The _____ approach is relatively new and not yet proven in market Place, but is often considered as an alternative to the SMP or cluster :->NUMA
35. SMP comes under _____ stream :->MIMD
36. In _____ stream, a set of processors simultaneously execute Different instruction sequence on different data sets :->MIMD
37. In _____ stream, a sequence of data is transmitted to a set Of processors,each of which executes a different instruction sequence :->MISD
38. Uniprocessor comes under _____ stream :->SISD
39. Clusters comes under _____ stream :->MIMD
40. NUMA comes under _____ stream:->MIMD
41. An SMP consists of multiple _____ within the same computer :->Processors
42. NUMA means _____ :->Non uniform memory access
43. SMP means _____ :->Symmetric multiprocessors
44. One of the most common multiprocessor organisations is _____ :->SMP
45. At the micro-operation level,multiple control signals are generated at the _____ :->Same time
46. _____ is a group of interconnected ,whole computers working together as a unified computing resource :->Cluster
47. The most critical problem to address in an SMP is that of _____ :->Cache coherence
48. _____ have become increasingly common to support Workloads that are beyond capacity to a single SMP :->Cluster
49. In an SMP organisation, multiple processors share a _____ :->Common memory
50. SMPs is example of _____ organisation:->Parallel
51. In _____ interrupt mode, interrupt requests are ordered in priority from 0(IR0) through 7(IR7). :->fully nested
52. With _____, an I/O module first gains control of the bus before it raises the interrupt request line. :->bus arbitration
53. In daisy chain method, the requesting module responds by placing a word on the data lines. This word is referred to as _____ :->vector
54. _____ method provides a hardware poll.:->daisy chain
55. The technique in which DMA module force the processor to suspend operation temporarily is _____. :->cycle stealing
56. _____ interrupt mode allows the processor to inhibit interrupts from certain devices. :->special mask
57. In which interrupt mode, a devices with equal priority are given lowest priority, after being serviced. :->rotating
58. _____ channel can handle I/O with multiple devices at the same time. :->multiplexor
59. _____ channel controls multiple high-speed devices and, at any one time, is dedicated to the transfer of data with one of those devices. :->nested
60. _____ causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral. :->write
61. _____ causes the I/O module to obtain an item of data from the peripheral and place it in an internal buffer. :->read
62. _____ I/O command is used by processor to know that the most recent I/O operation is completed and if any errors occurred. :->test
63. _____ I/O command used to activate a peripheral and tell it what to do. :->control
64. With _____, the address space for I/O is isolated from that for memory. :->isolated I/O

65. With memory-mapped I/O, a single _____ line and a single _____ line are needed on the bus. :->read, write
66. With _____, there is a single address space for memory locations and I/O devices. :->memory-mapped I/O
67. For which method it is impractical to dedicate more than a few bus lines or processor pins to interrupt lines. :->multiple interrupt lines
68. The process in which the processor detects an interrupt, and branches to an interrupt-service routine whose job is to poll each I/O module to determine which module caused the interrupt. :->software poll
69. For _____ there are only a few I/O instructions. :->isolated I/O
70. The I/O function includes a _____ requirement, to coordinate the flow of traffic between internal resources and external devices. :->Control and timing
71. _____ indicates that the code combinations that follow shall be interpreted according to the standard character set. :->SI
72. _____ indicates the end of a transmission, which may have included one or more "texts" with their headings. :->EOT
73. _____ indicates movement of the printing mechanism or display cursor to the starting position of the same line. :->CR
74. An I/O module is often responsible for _____. :->error detection
75. An essential task of an I/O module is _____. :->data buffering
76. Processor Communication does not involve _____. :->data buffering
77. _____ requires interrupts in direct-I/O-to memory transfer. :->direct memory access
78. I/O controllers are commonly seen on _____ whereas I/O channels are used on _____. :->microcomputers, mainframes
79. The processor uses the _____ to issue commands to the I/O module. :->control lines
80. _____ signals indicate the state of the device. :->status
81. _____ are in the form of set of bits to be sent to or received from the I/O module. :->data
82. _____ signals determine the function that the device will perform, such as send data to the I/O module. :->control
83. _____ to the I/O module is in the form of control, data and status signals. :->interface
84. The basic unit of exchange is _____. :->character
85. The _____ converts data from electrical to other forms of energy during output and from other forms to electrical during input. :->transducer
86. _____ logic associated with the device controls the device's operation in response to direction from the I/O module. :->control
87. _____ indicates movement of the printing mechanism or display cursor to the starting position of the next page, form or screen. :->FF
88. The most commonly used text code is _____. :->international reference alphabet
89. Associated with each character is the code, typically _____ or _____ bits of length. :->7 or 8
90. _____ in which a program issues an I/O command and then continues to execute, until it is interrupted by the I/O hardware to signal the end of the I/O operation. :->interrupt driven I/O
91. _____ in which I/O occurs under the direct and continuous control of the program requesting the I/O operations. :->programmed I/O
92. There are _____ principal I/O techniques. :->three
93. The computer system's I/O architecture is _____ to the outside world. :->interface
94. The _____ is used to exchange control, status and data between the I/O module and the external device. :->link
95. Each I/O module interfaces to the _____ and controls one or more peripheral devices. :->system bus
96. _____ in which a specialized I/O processor takes over control of an I/O operation to move a

large block of data :->direct memory access

97. _____ devices are suitable for communicating with the remote devices:->communication
98. _____ devices are suitable for communicating with the equipment:->machine readable
99. _____ devices are suitable for communicating with the computer user:->human readable
100. DQ0 in SDRAM pin assignments represents _____ :->data input/output
101. \overline{WE} in SDRAM pin assignments represents _____ :->write enable
102. \overline{CAS} in SDRAM pin assignments represents _____ :->column address strobe
103. In SDRAM pin assignments \overline{RAS} represents _____ :->row address strobe
104. RDRAM developed by Rambus has been adopted by _____ for its Pentium and Itanium processors. :->Intel
105. DQM in SDRAM pin assignments represents _____ :->data mask
106. DQ7 in SDRAM pin assignments represents _____ :->data input/output
107. A _____ is a random, non-destructive event that alters the contents of one or more memory cells, without damaging the memory.:->soft error
108. A _____ is a permanent physical defect so that the memory cell affected cannot reliably store data. :->hard failure
109. Cache DRAM is developed by _____ :->Mitsubishi
110. When only a small number of ROMs with a particular memory content is needed :->PROM
111. An important application of ROM is _____ :->micro programming
112. _____ is not possible in ROM. :->write new data
113. A ROM is _____ :->non-volatile
114. In SDRAM pin assignments A0 represents _____ :->address input
115. In SDRAM pin assignments A4 represents _____ :->address input
116. PROM is _____ :->non-volatile
117. In SDRAM pin assignments, \overline{CS} represents _____ :->chip select
118. In SDRAM pin assignments CKE represents _____ :->clock enable
119. In SDRAM pin assignments CLK represents _____ :->clock input
120. In DRAM, the address line is used to open or close a _____ :->Switch
121. A typical SRAM will hold its data as long as _____ is supplied to it.:->Power
122. In a SRAM, binary values are stored using traditional _____ logic-gate Configurations. :->Flip-Flop
123. Flash memory comes under _____ category:->Read-Mostly Memory
124. DRAM is _____ than a SRAM:->Smaller
125. DRAM is _____ than a SRAM :->Simpler
126. Both static and dynamic RAMs are _____ :->Volatile
127. ROM contains a _____ pattern of data.:->permanent
128. DRAM is _____ than a SRAM :->More Dense
129. Smaller cells = _____ :->More Cells per unit area
130. A DRAM is made with cells that store data as charge on _____ :->Capacitor
131. The two traditional forms of RAM used in computers are DRAM and _____ :->SRAM
132. RAM can be used only as a _____ storage:->Temporary
133. The distinguishing characteristic of RAM is _____ :->Volatile
134. ROM comes under _____ category:->Read-Only Memory
135. RAM comes under _____ category :->Read-Write Memory
136. The presence and absence of a charge on capacitor is interpreted as a binary _____ :->1 or 0
137. EEPROM comes under _____ category:->Read-Mostly Memory
138. EPROM comes under _____ category :->Read-Mostly Memory

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139. PROM comes under _____ category:-->Read-Only Memory
140. Both synchronous DRAM and Rambus DRAM involve using the _____ to Provide for transfer of blocks of data. :-->System clock
141. Error correction systems are commonly used in _____ :-->Memory Systems
142. _____ is used for main memory:-->DRAM
143. _____ is used for cache memory. :-->SRAM
144. Memory cell has _____ functional terminals :-->Three
145. Semi conductor memory cells exhibit _____ stable states :-->Two
146. In earlier computers, main memory was often referred to as _____ :-->Core
147. The _____ terminal indicates read or write:-->Control
148. The select terminal, as the name suggests, selects a memory cell for a _____ Operation. :-->Read and Write
149. The memory cell has three functional terminals capable of carrying an _____ :-->Electrical Signal
150. Signed divide is iterate function of _____ :-->SDIVI
151. Cyclic redundancy character accum is function of _____ :-->CRC
152. Test bit1 is function of _____ :-->TB1
153. Byte increment S is function of _____ :-->BINCS
154. _____ refers to the use of a micro program on one machine to execute program originally Written for another :-->Emulation
155. Excess-3 byte connection is function of _____ :-->EX3BC
156. Signed divide terminate is function of _____ :-->SDIVIT
157. The LSI-11 makes use of a _____ bit micro instruction and control memory of 2k 22-bit Word :-->22
158. The Texas instruments 8800 software development board is a micro programmable _____ on Computer card :-->32
159. The principal function of 8818 micro sequences is to generate next _____ the micro Processor :-->Micro instruction addresses
160. In Wilkes model, the heart of the system is a matrix particularly filled with _____ :-->diodes
161. In wilkes model the heart of the system is a _____ particularly filled with diodes :-->matrix
162. Wilkes first proposed use of a micro programmed control unit in _____ :-->1951
163. The advantage of vertical micro instructions is there are more _____ :-->compact
164. Arithmetic right single precision shift is a function _____ :-->SRA
165. In wilkes model the first part of the low generate the control signal, that control the operation Of the _____ :-->processor
166. In wilkes model using a machine cycle, one low of the matrix is activated with a _____ :-->pulses
167. Arithmetic left double precision shift is function of _____ :-->SLAD
168. Subtract immediate is a function of _____ :-->SUB1
169. Circular left shift MQ register is function of _____ :-->MQSLC
170. The sequencing _____ loads a new address into the control address register :-->Logic unit
171. The content of the _____ generates control signal :-->Control buffer register
172. The word whose address is specified in the control address register is read into _____ :-->Control buffer register
173. To execute an instruction, the sequencing logic unit issues a _____ command to the Control memory :-->READ
174. The _____ decoder translates the op-code of the IR into a control memory address :-->Upper
175. The sequencing logic unit loads a _____ into the control address register :-->new address
176. In horizontal micro instructions every bit in the control field attached to a _____ :-->Control line
177. The _____ decoder used for vertical micro instructions :-->Lower
178. The _____ decoder is not used for horizontal micro instructions :-->Lower

179. There is field with the _____ of the micro instruction to the executed next when a Branch is taken :->**data**
180. There is a _____ indicating the condition under which there should be a branch :->**Condition field**
181. In format of micro instructions, there is _____ for each system bus control unit :->**one bit**
182. In format of micro instruction, there in _____ for each internal processor control line :-> **one bit**
183. In control memory, each routine ends with a _____ instruction indicating where to go Next :->**Jump**
184. In control memory, each continue ends with a instruction indicating where to go next :->**branch**
185. The micro instructions in each routine are to be executed :->**parallel**
186. When a micro instruction is read from the control memory it is transferred to a _____ :->**Control buffer register**
187. The _____ register contains the address of the next micro instruction to be read :->**control address register**
188. The set of micro instructions is stored in _____ :->**control memory**
189. A micro programmed control unit is a relatively simple logic circuit that is capable of sequencing through _____ :->**Micro instructions**
190. Micro programming instructions specifies _____ :->**Micro operations**
191. A micro program consists of sequence of instructions in _____ language :->**micro programming**
192. Micro programmed control unit in which the logic of the control unit is specified by a _____ :->**micro program**
193. The control signals generated by micro instructions are used to cause _____ :->**register transfer**
194. A micro programmed control unit is capable of generating _____ to execute each micro instructions :->**code**
195. A micro programmed control unit is a relatively simple _____ :->**Logic circuit**
196. _____ is midway between hardware and software :->**micro program**
197. The term 'micro program' was first caused by _____ :->**M.V wilkes**
198. The control signals generated by micro instructions are used to cause _____ :->**ALU operation**

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